

Industrial M.2 2242 SATA3 SSD MDA3K0E Series Datasheet



Specifications Overview

- **Capacity**
 - 64GB, 128GB, 256GB, 512GB, 1TB
- **Form Factor**
 - M.2 2242 standard
- **Interface**
 - SATA III
- **Performance**
 - Sequential Read: up to 540 MB/s
 - Sequential Write: up to 520 MB/s
 - Random 4k Read: up to 44K IOPS
 - Random 4k Write: up to 69K IOPS
- **Temperature Range**
 - Operation temperature:
Normal temperature: -20°C to +75°C
 - Storage temperature: -40°C to +85°C
- **Power Consumption**
 - Supply Voltage: DC +3.3V ± 5%
 - Read (Max.): 315 mA
 - Write (Max.): 360 mA
 - Idle (Avg.): 90 mA
- **Reliability**
 - TBW:
64GB: 86TB
128GB: 171TB
256GB: 342TB
512GB: 684TB
1TB: 1,369TB
 - MTBF: > 3,000,000 hrs
- **ECC Performance**
 - Hardware LDPC
- **Environment Specification**
 - Shock
 - Vibration
- **Compliant Specifications**
 - RoHS 2.0
- **Feature Support**
 - AES
 - Write Protect
 - Quick Erase

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Revision History

Revision	Date	Major Changes
	2022/02/16	1. Preliminary
1.0	2022/11/14	1. First Release
1.1	2023/09/25	1. Update order information
1.2	2023/11/14	1. Update temperature specification
1.3	2024/06/05	1. Add 064GIMDA3K5EV0-040 2. Add 128GIMDA3K5EV0-040 3. Add 256GIMDA3K5EV0-030 4. Add 512GIMDA3K5EV0-030 5. Add 010TIMDA3K5EV0-020

1. Product Description

1.1 Overview

Silicon Power's MDA3K0E series M.2 2242 SATA3 solid state is a storage device based on 3D NAND flash memory technology. The MDA3K0E series includes the following models to fulfill a variety of different demands: MDA3K0E Embedded series – DRAM-less and power-shielding firmware architecture protection to manage sudden power-loss situations.

The MDA3K0E series is equipped with advanced LDPC ECC engine to correct up to 2KB code word, as well as a Block/Page RAID function to guarantee 3K PE cycles endurance with 3D NAND. It also features the latest Direct-To-TLC and Dynamic SLC cache firmware architecture to achieve the optimal sustained read/write performance and reduce Write Amplification to offer even better TBW endurance than 2D MLC models can offer.

Early weak block retirement and global wear leveling algorithm assures an equal usage of the flash memory cells to extend SSD lifespan. The MDA3K0E series contains hardware write protection and a quick erase function via an optional specific pin. It can also provide software write protection and a Quick Erase function via vendor commands, by request.

The MDA3K0E series is equipped with an Industrial-grade circuit design to provide a higher reliability power design compared to traditional discrete circuits. It also features complete protection with OVP, OCP, Surge Rejection, and In-Out Short Protection to provide a higher level of protection versus traditional fuse design.

1.2 Features

- M.2 2242 standard form factor with Serial ATA standard interface connector.
- Compliant with Serial ATA revision 3.1 standard with 6.0 Gb/s transfer rate.
- Compliant with ATA/ATAPI-8 standard and ACS-3 command protocol.
- Built-in-Voltage detector for power shielding protection and an advanced PFP function
- Native Command Queuing up to 32 commands
- Garbage collection and TRIM Data Set Management command
- Global wear leveling algorithm evens program/erase count
- Early weak block retirement
- Supports SMART feature command set.
- Supports 28/48 bit LBA mode command
- Supports SATA DEVSLP for advanced power saving.
- Built-in temperature sensor (Thermal Throttling) function to adjust access speed of NAND flash and keep the SSD system stable.
- Supports real time Full Disk Encryption (FDE) with Advanced Encryption Standard (AES) 128/256-bit strength.
- Supports JTAG, UART, and I2C interface for on-system debug service (optional service).
- Supports in-field seamless FW update tool via USB interface to keep the SSD's original data (optional service).

1.3 System Requirements

- SATA 6.0 Gb/s Interface, backward compatible with 1.5/3.0 Gb/s, with M.2 2242 standard form factor.
- Voltage: DC +3.3V ± 5%
- Operating System:
 - Windows
 - Linux
 - DOS

2. Specification

2.1 Physical Dimension

2.1.1 Dimension

The dimensions of M.2 2242 SATA3 SSD are illustrated in Figure 1 and described in Table 1.

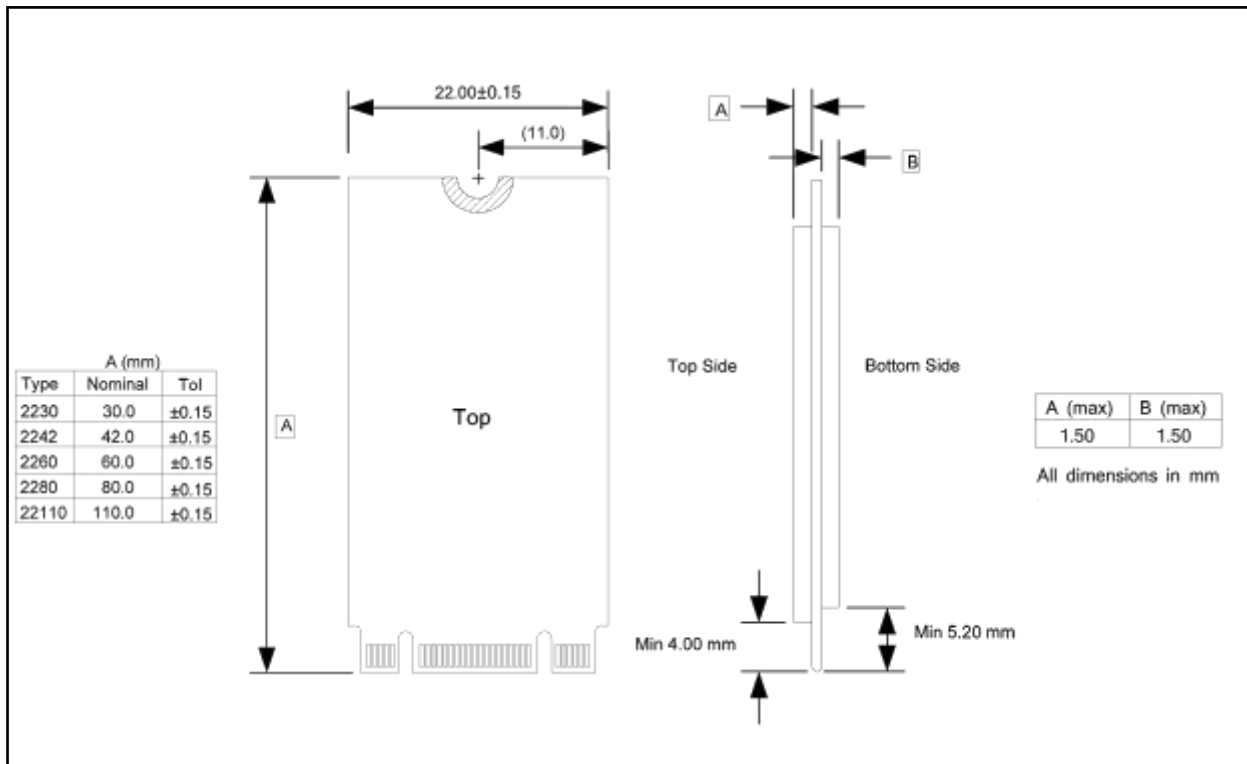


Figure 1 : M.2 2242 SATA3 SSD Dimensions

Table 1 : M.2 2242 SATA3 SSD Physical Dimension

Length	42±0.15mm
Width	22±0.15mm
Thickness(connector)	3.5mm

2.1.2 Weight

- 64GB: 3.10g ± 5%
- 128GB: 3.18g ± 5%
- 256GB: 3.60g ± 5%
- 512GB: 3.63g ± 5%
- 1TB: 3.70g ± 5%

2.2 Electrical Specifications

2.2.1 Operating Condition

- Supply Voltage: DC +3.3V ± 5%

Table 2 : Power Consumption

Mode	Power Consumption					Unit
	64GB	128GB	256GB	512GB	1TB	
Read (Max.)	250	310	310	315	315	mA
Write (Max.)	265	335	350	360	360	mA
Idle (Avg.)	< 90	< 90	< 90	< 90	< 90	mA

Notice: The value is various bases on the capacity and the test platform.

Notice: Power consumption is measured during the sequential read and write operations performed by CrystalDiskMark.

Notice: Power consumption of Idle is measured when the platform gets into a steady-state mode after IOMeter runs "Idle" script for 10mins..

※Testing Platform: Test PC: MSI-Z87-G45 GAMING, CPU: Intel(R) Dual-Core i5-4430 CPU 3.0GHz, Memory: DDR3-1600 2GB X 2pcs, Testing OS: Windows 7 32 Bit, Testing Software: Crystal Disk Mark 5.5.0

2.2.2 External DRAM information (MDA3K0E series)

- N/A

2.2.3 LED signal definitions

- D2 : Controller Activity – to indicate the controller working status
- D1 : Data activity to SATA interface – to indicate the data access activity on SATA interface

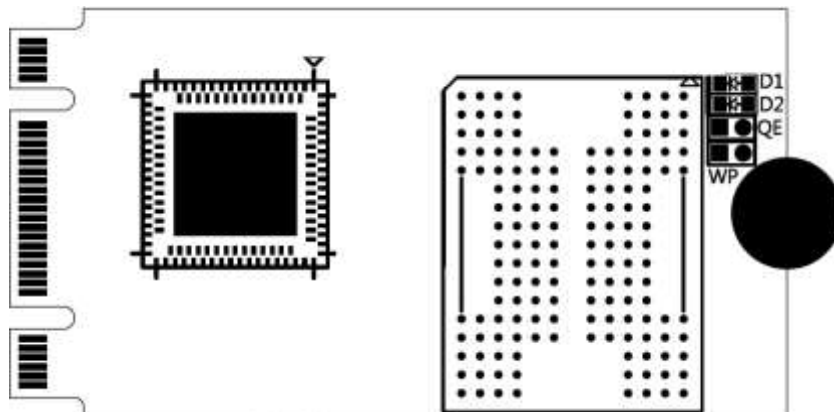


Figure 2 : M.2 2242 SATA3 SSD LED indicator

2.3 Performance

2.3.1 Transfer Modes

- Serial ATA 6.0 Gb/s, backward compatible with Serial ATA 1.5/3.0 Gb/s.

2.3.2 Data Access Performance

- Maximum Sequential Access

Mode	Maximum Sequential Access					Unit
	64GB	128GB	256GB	512GB	1TB	
Read	295	540	545	545	540	MB/s
Write	240	480	520	520	515	MB/s

Notice: The value is various bases on the capacity and the test platform.

Notice: Test Platform: Average Value is based on Serial ATA 6.0Gb/s interface.

※Testing Platform: Mother-Board MSI-Z87-G45 GAMING, CPU: Intel(R) Dual-Core i5-4430 CPU 3.0GHz, Memory: DDR3-1600 2GB X 2pcs, Operating System: Win 7, 32bit, Testing Software: CrystalDiskMark5.5.0

- Maximum 4K Random Access

Mode	Maximum 4K Random Access (QD32)					Unit
	64GB	128GB	256GB	512GB	1TB	
Read	9,000	18,000	31,000	44,000	44,000	IOPS
Write	54,000	67,000	67,000	68,000	69,000	IOPS

Notice: The value is various bases on the capacity and the test platform.

Notice: Test Platform: Average Value is based on Serial ATA 6.0Gb/s interface.

※Test Platform: Mother-Board MSI-Z87-G45 GAMING, CPU: Intel(R) Dual-Core i5-4430 CPU 3.0GHz, Memory: DDR3-1600 2GB X 2pcs, Operating System: Win 7, 32bit, Testing Software: CrystalDiskMark5.5.0

2.3.3 TeraByte Write

Table 3 : TBW Data

Mode	TBW Data					Unit
	64GB	128GB	256GB	512GB	1TB	
Client	86	171	342	684	1369	TB
Enterprise	28	56	111	222	444	TB

Notice: TBW is estimated by formula $TBW = (\text{Capacity} \times \text{PE Cycles}) \times (1 + \text{OP}) \times (\text{WLE}) / (\text{WAF})$

- **OP = (Physical Capacity / Logical Capacity) - 1**
- **WLE** = It could be different depended on the workload or usage containing data size and access rate.
- **Client workload:** Sequential write workload which is generated by VDBENCH script and tested by VDBENCH.
- **Enterprise workload:** Follow JESD219A enterprise workload which is generated by VDBENCH script and tested by VDBENCH.

2.3.4 Wear-Leveling

- Enhanced endurance by global Wear-Leveling.

2.4 Environmental Conditions

Table 4 : Environmental Conditions

Feature	Operating	Non-Operating
Temperature (Normal Grade)	-20°C to +75°C	-55°C to +95°C
Humidity	10% to 95% RH, non-condensing	
Vibration	20G (Peak-to-Peak), 80~2000 Hz	
Shock	1,500G, 0.5ms	

Notice:

- Vibration: Duration, 30 min x 3 axis.
- Shock: 1500G, 0.5msec, half-sine wave, 3 times in each direction, total = 18 times (6 directions).
- Temperature: The temperature reading is for the environment defined as Ta.

2.5 Reliability

Table 5 : Reliability

Feature	Specification
ECC Capability	Hardware LDPC ECC engine (120bit/1KB) and Block/Page RAID
MTBF	>3,000,000 hrs @25°C (MIL-HDBK-217F part count method Telcordia SR-332 Method)
Program / Erase Endurance	3,000 P/E cycles
Optimal sustained performance	Direct-To-TLC and SLC Cache Architecture
Data Endurance & Data integrity	StaticDataRefresh technology, Early weak block retirement, Global Wear leveling
Data Retention	10% of program / Erase Endurance cycles: 10 Years
	100% of program / Erase Endurance cycles: 1 Years

Notice:

- Data retention: The value is based on normal program/erase endurance at room temperature. High environmental temperature may shorten the retention period.

2.6 Compliance Specifications

- CE (EN55032 & EN55035)
- FCC Part 15, subpart B
- RoHS 2.0 (2011/65/EU & 2015/863/EU)

2.7 Technique

2.7.1 Write Protect

The Industrial SSD contains a feature connector for Write Protect mode. Write Protect mode is enabled when the Write Protect feature connector is placed at 1.27mm pitch Pin Header after power up or any time. During Write Protect mode, the SSD is read-only and data can't be written to it. If no feature connector is placed, data can be written as usual.

2.7.2 Quick Erase

Reliably erasing data from storage media is a critical component of secure data management. Flash-based solid-state drives (SSDs) differ from hard drives in both the technology they use to store data (flash chips vs. magnetic disks) and the algorithms they use to manage and access that data. SSDs maintain a layer of indirection between the logical block addresses that computer systems use to access data and the raw flash addresses that identify physical storage. The layer of indirection enhances SSD performance and reliability by hiding the flash memory's idiosyncratic interface and managing its limited lifetime. However, it can also produce copies of the data that are invisible to the user but recoverable by a sophisticated attacker. For this reason, it is so important to sanitize the media completely.

2.7.3 Power Shield

The principle of SSD is Power Shield (PS) activates when the external voltage drops to a specific low level, such as from 3.3V to 2.7V. The voltage detection circuit (Voltage Detector) inside the controller will initiate the power supply protection function. When the SSD is operating and the DRAM is powered by an external power supply, the data will be temporarily stored in the DRAM. During the power-off process, the command is sent from the host to the SSD controller to signal that the power is about to be interrupted, and the SSD controller will send confirmation messages to the host, and then transfer the data temporarily stored in the DRAM cache to the Flash Memory. This safeguards the internal firmware and data of the Flash memory from being damaged.

2.7.4 Bad Block Management

Bad Block Management is a mechanism for bad blocks implemented by the controller to detect and mark the bad blocks in the flash memory, and it uses reserved spare blocks to replace the bad blocks to prevent the data from being written into the bad block again. Bad Block Management improves the reliability and endurance of data access.

2.7.5 Garbage Collection

SSD uses the storage technology of flash memory (NAND flash). The principle of SSD is that the controller stores the data to be written in the Flash memory. When writing data, the SSD must first erase the data in the old block before writing new data. That is, the new data cannot directly cover the old invalid data. For SSD, Garbage Collection refers to the process of re-transferring existing data to other NAND flash locations and erasing useless data.

2.7.6 Wear Leveling

For today's NAND flash devices, the main limitation is Program/Erase lifespan (number of P/E cycles). The key solution for this constraint is to manage the attrition rate in the entire NAND flash device so that each block will be evenly distributed. Therefore, efficient management of wear in whole blocks is required in order to maximize the lifespan of a NAND flash device. To accomplish this, one method is to manage the P/E cycle of each block individually, which will help to regularly distribute them and avoid overlaying on some blocks. This method is called wear leveling.

3. Functional Description

3.1 Architecture

SILICON POWER's M.2 2242 SATA3 SSD MDA3K0E series is designed to operate and work as data or code storage device by NAND Flash memory and its controller through Standard Serial ATA 6.0Gb/s interface to host systems.

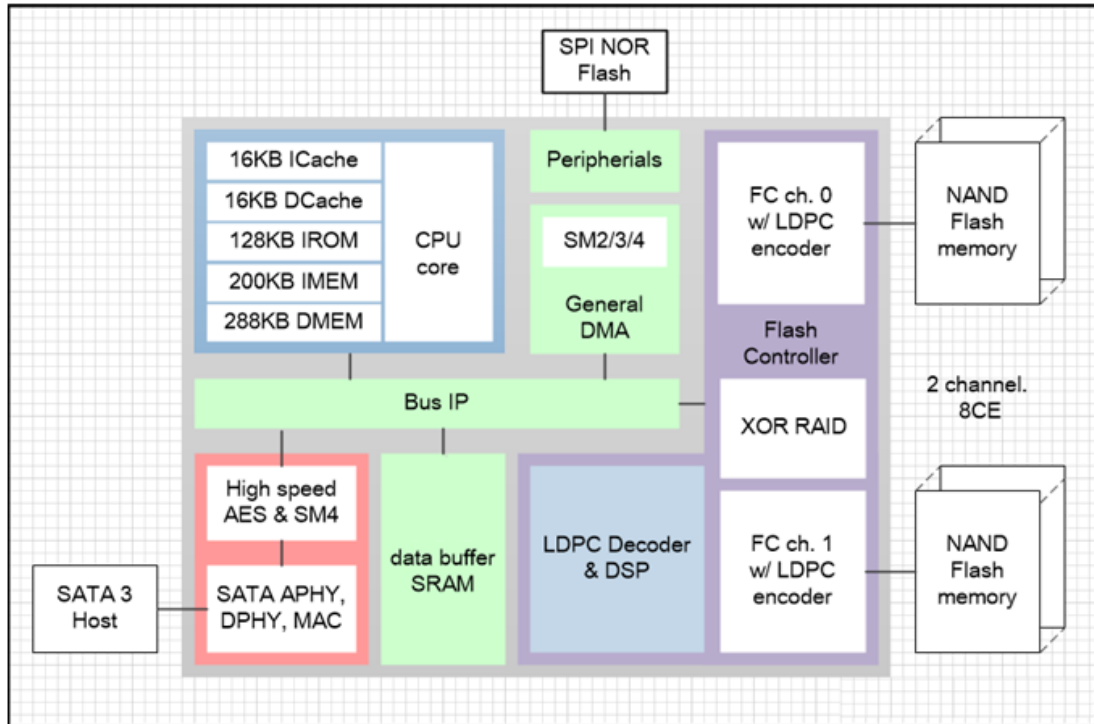


Figure 3 : M.2 2242 SATA3 SSD Block Diagram

3.2 Signal Assignment

Pin No.	Signal Name	Key	Pin No.	Signal Name	Key
2	3.3V	B	1	CONFIG_3	B
4	3.3V	B	3	CONFIG_0	B
6	3.3V	B	5	CONFIG_1	B
8	NA	B	7	CONFIG_2	B
10	NA	B	9	CONFIG_3	B
	DAS/DSS	B	11	CONFIG_0	B
20	NA	M	21	CONFIG_1	M
22	NA	M	23	CONFIG_2	M
24	NA	M	25	CONFIG_3	M
26	NA	M	27	CONFIG_0	M
28	NA	M	29	CONFIG_1	M
30	NA	M	31	CONFIG_2	M
32	NA	M	33	CONFIG_3	M
34	NA	M	35	CONFIG_0	M
36	NA	M	37	CONFIG_1	M
38	NA	M	39	CONFIG_2	M
40	DEVSLP	M	41	CONFIG_3	M
42	NA	M	43	CONFIG_0	M
44	NA	M	45	CONFIG_1	M
46	NA	M	47	CONFIG_2	M
48	NA	M	49	CONFIG_3	M
50	NA	M	51	CONFIG_0	M
52	PERST#	M	53	CONFIG_1	M
54	CLKREQ#	M	55	CONFIG_2	M
56	PEWAKE#	M	57	CONFIG_3	M
58	MFG_1	M			
	MFG_2	M			
	REFCLK_N	M			
	REFCLK_P	M			
	REFCLK_GND	M			
	SATA-A+	M			
	SATA-A-	M			
	SATA-B+	M			
	SATA-B-	M			
	SATA-GND	M			
	SATA-A+	M			
	SATA-A-	M			
	SATA-B+	M			
	SATA-B-	M			
	SATA-GND	M			
	SATA-A+	M			
	SATA-A-	M			
	SATA-B+	M			
	SATA-B-	M			
	SATA-GND	M			
68	SUSCLK	M	67	NA	M
70	3.3V	M	69	CONFIG_1	M
72	3.3V	M	71	CONFIG_2	M
74	3.3V	M	73	CONFIG_3	M
76	3.3V	M	75	CONFIG_0	M
	TOP HOLE	M			

Figure 4 : SATA Signal Connector

Table 6 : M.2 SSD Serial ATA connector pin definitions

Definition	Name	Pin No		Name	Definition
Ground	CONFIG_3	01	02	+3.3V	Supply pin, 3.3 V
Ground	GND	03	04	+3.3V	Supply pin, 3.3 V
No connect	NC	05	06	Not available	No Connect
No connect	NC	07	08	NC	No Connect
No connect	NC	09	10	DAS/DSS	Device Activity Signal / Disable Staggered Spinup
No connect	NC	11	12	Module Key	Mechanical notch B
Mechanical notch B	Module Key	13	14	Module Key	Mechanical notch B
Mechanical notch B	Module Key	15	16	Module Key	Mechanical notch B
Mechanical notch B	Module Key	17	18	Module Key	Mechanical notch B
Mechanical notch B	Module Key	19	20	Not Available	No Connect
Ground	CONFIG_0	21	22	Not available	No Connect
No Connect	Not available	23	24	Not available	No Connect
No Connect	Not available	25	26	Not available	No Connect
Ground	GND	27	28	Not available	No Connect
No Connect	Not available	29	30	Not available	No Connect
No Connect	Not available	31	32	Not available	No Connect
Ground	GND	33	34	Not available	No Connect
No Connect	Not available	35	36	Not available	No Connect
No Connect	Not available	37	38	DEVSLP	Device Sleep
Ground	GND	39	40	Not available	No Connect
Host receiver differential signal pair of SSD	SATA B+	41	42	Na	No Connect
Host receiver differential signal pair of SSD	SATA B-	43	44	Not available	No Connect
Ground	GND	45	46	Not available	No Connect
Host transmitter differential signal pair of SSD	SATA A-	47	48	NC	No Connect
Host transmitter differential signal pair of SSD	SATA A+	49	50	PERST#	No Connect
Ground	GND	51	52	NC	No Connect
No Connect	NC	53	54	NC	No Connect
No Connect	NC	55	56	Reserved	No Connect
Ground	GND	57	58	Reserved	No Connect
Mechanical notch M	Module Key	59	60	Module Key	Mechanical notch M
Mechanical notch M	Module Key	61	62	Module Key	Mechanical notch M
Mechanical notch M	Module Key	63	64	Module Key	Mechanical notch M

Mechanical notch M	Module Key	65	66	Module Key	Mechanical notch M
No Connect	NC	67	68	SUSCLK	No Connect
Ground	CONFIG_1	69	70	+3.3V	Supply pin, 3.3 V
Ground	GND	71	72	+3.3V	Supply pin, 3.3 V
Ground	GND	73	74	+3.3V	Supply pin, 3.3 V
Ground	CONFIG_2	75			

NOTICE: DEVSLP function is depended on Host supporting.

3.3 Support ATA Commands

The table showed below summarizes the supported ATA command set. For detail description of the commands, please check the ATA standard or contact Silicon Power local representatives for the helps.

Table 7 : ATA Command Set

No	Command Set	Code	FR	SC	SN	CY	DH	LBA
General Feature Set								
1	Execute Drive Diagnostic Mode	90h	-	-	-	-	D	-
2	Flush Cache	E7h	-	-	-	-	D	-
3	Identify Device	ECh	-	-	-	-	D	-
4	Initialize Device Parameters	91h	-	Y	-	-	Y	-
5	NOP	00h	-	-	-	-	D	-
6	Read Buffer	E4h	-	-	-	-	D	-
7	Read DMA	C8h	-	Y	Y	Y	Y	Y
8	Read Multiple	C4h	-	Y	Y	Y	Y	Y
9	Read Sector(s)	20h	-	Y	Y	Y	Y	Y
10	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
11	Seek	7xh	-	Y	-	Y	Y	Y
12	Set Feature	EFh	Y	-	-	-	D	-
13	Set Multiple Mode	C6h	-	Y	-	-	D	-
14	Write Buffer	E8h	-	-	-	-	D	-
15	Write DMA	CAh	-	Y	Y	Y	Y	Y
16	Write Multiple	C5h	-	Y	Y	Y	Y	Y
17	Write Sector(s)	30h	-	Y	Y	Y	Y	Y
48-bit Address Feature Set								
18	Flush Cache Ext	EAh	-	-	-	-	D	-
19	Read DMA Ext	25h	-	Y	Y	Y	Y	Y
20	Read Multiple Ext	29h	-	Y	Y	Y	Y	Y
21	Read Sector(s) Ext	24h	-	Y	Y	Y	Y	Y
22	Read Verify Sector(s) Ext	42h	-	Y	Y	Y	Y	Y
23	Write DMA Ext	35h	-	Y	Y	Y	Y	Y
24	Write DMA FUA Ext	3Dh	-	Y	Y	Y	Y	Y
25	Write Multiple Ext	39h	-	Y	Y	Y	Y	Y
26	Write Multiple FUA Ext	CEh	-	Y	Y	Y	Y	Y
27	Write Sector(s) Ext	34h	-	Y	Y	Y	Y	Y
Host Protected Area (HPA) Feature Set (Option)								
28	Read Native Max Address	F8h	-	-	-	-	D	-
29	Read Native Max Address Ext	27h	-	-	-	-	D	-
30	Set Max Address	F9h	-	Y	Y	Y	Y	Y
31	Set Max Address Ext	37h	-	Y	Y	Y	Y	Y
32	Set Max Freeze Lock	F9h	04h	-	-	-	D	-
33	Set Max Lock	F9h	02h	-	-	-	D	-
34	Set Max Set Password	F9h	01h	-	-	-	D	-
35	Set Max Unlock	F9h	03h	-	-	-	D	-
Power Management Feature Set								
36	Check Power Mode	E5h or 98h	-	-	-	-	D	-
37	Idle	E3h or 97h	-	Y	-	-	D	-
38	Idle Immediate	E1h or 95h	-	-	-	-	D	-
39	Sleep	E6h or 99h	-	-	-	-	D	-
40	Standby	E2h or 96h	-	-	-	-	D	-
41	Standby Immediate	E0h or 94h	-	-	-	-	D	-
Security Mode Feature Set								

No	Command Set	Code	FR	SC	SN	CY	DH	LBA
42	Security Disable Password	F6h	-	-	-	C	-	-
43	Security Erase Prepare	F3h	-	-	-	C	-	-
44	Security Erase Unit	F4h	-	-	-	C	-	-
45	Security Freeze Lock	F5h	-	-	-	C	-	-
46	Security Set Password	F1h	-	-	-	C	-	-
47	Security Unlock	F2h	-	-	-	C	-	-
SMART Feature Set								
48	SMART Disable Operations	B0h	D9h	Y	-	Y	Y	-
49	SMART Enable/Disable Autosave	B0h	D2h	Y	-	Y	Y	-
50	SMART Enable Operations	B0h	D8h	Y	-	Y	Y	-
51	SMART Execute Off-Line Immediate	B0h	D4h	Y	-	Y	Y	-
52	SMART Read Data	B0h	D0h	Y	-	Y	Y	-
53	SMART Read Threshold	B0h	D1h	Y	-	Y	Y	-
54	SMART Return Status	B0h	DAh	Y	-	Y	Y	-
55	SMART Save Attribute Values	B0h	D3h	Y	-	Y	Y	-

Definitions:

FR = Features register **SN** = Sector number register **DH** = Device/drive/head register

CY = Cylinder registers **SC** = Sector count register **D** = Only the device parameter is valid and not the head parameter

LBA = Logical block address mode supported (see command descriptions for use).

Y - The register contains a valid parameter for this command. For the drive/head register Y means both the device and head parameters are used.

C - The register contains command specific data (see command descriptions for use).

3.4 Device Identification

This command read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

Table 8 : Identify Device Information

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information
0	0044h	2	F X F X X F X F	General configuration – Bit Significant with ATA definitions. 15 0:ATAdevice 14-8 Retired 7 1:removablemediadevice 6 Obsolete 5-3 Retired 2 Response incomplete 1 Retired 0 Reserved
1	XXXXh	2	X	Default number of cylinders
2	0000h	2	V	Reserved
3	00XXh	2	X	Default number of heads
4-5	XXXXh	4	X	Reserved
6	XXXXh	2	X	Default number of sectors per track
7-8	XXXXh	4	V	Reserved for assignment by the CFA
9	0000h	2	X	Reserved
10-19	Aaaa	20	F	Serial number in ASCII (Right Justified)
20-21	XXXXh	4	X	Reserved
22	XXXXh	2	X	Reserved
23-26	aaaa	8	F	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	F	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	8001h	2	F F	Maximum number of sectors on Read/Write Multiple command 15-8 80h: Fixed 7-0 00h: Reserved 01h: Maximum number of 1 sectors on READ/WRITE MULTIPLE commands
48	XXXXh	2	X	Reserved
49	0F00h	2	F F F F F F F X	Capabilities: DMA, LBA, IORDY supported 15-14 Reserved for the IDENTIFY PACKET DEVICE command. 13 1: Standby timer values as specified in this standard are supported 0: Standby timer values shall be managed by the device 12 Reserved for the IDENTIFY PACKET DEVICE command 11 1: IORDY supported 0: IORDY may be supported 10 1: IORDY may be disabled 9 1: LBA supported 8 1: DMA supported 7-0 Retired

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information
50	4000h	2	F F F X F	Capabilities: Others, Fixed 15 Shall be cleared to zero. 14 Shall be set to one. 13-2 Reserved. 1 Obsolete 0 Shall be set to one to indicate a device specific Standby timer value minimum
51	0200h	2	X X	PIO data transfer cycle timing mode 2 15-8 PIO data transfer cycle timing mode 7-0 Reserved
52	XXXXh	2	X	Reserved
53	0007h	2	F F F X	Data Fields 54 to 58, 64 to 70 and 88 are valid 15-3 Reserved 2 1: the fields reported in word 88 are valid 0: the fields reported in word 88 are not valid 1 1: the fields reported in words 70:64 are valid 0: the fields reported in words 70:64 are not valid 0 1: the fields reported in words 58:54 are valid 0: the fields reported in words 58:54 are not valid
54	XXXXh	2	X	Current numbers of cylinders
55	00XXh	2	X	Current numbers of heads
56	XXXXh	2	X	Current sectors per track
57-58	XXXXh	4	X	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	0100h	2	F V V	Multiple sector setting 15-9 Reserved 8 1: Multiple sector setting is valid 7-0 xxh: Setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	XXXXh	4	F	Total number of sectors addressable in LBA Mode
62	0000h	2	X	Reserved
63	0007h	2	F V V V F F F F	Multiword DMA transfer. 15-11 Reserved 10 1: Multiword DMA mode 2 is selected 0: Multiword DMA mode 2 is not selected 9 1: Multiword DMA mode 1 is selected 0: Multiword DMA mode 1 is not selected 8 1: Multiword DMA mode 0 is selected 0: Multiword DMA mode 0 is not selected 7-3 Reserved 2 1: Multiword DMA mode 2 and below are supported 1 1: Multiword DMA mode 1 and below are supported 0 1: Multiword DMA mode 0 is supported

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information
64	0003h	2	F F	Advanced PIO modes 3 and 4 supported 15-8 Reserved 7-0 Advanced PIO modes supported
65	0078h	2	F	Minimum Multiword DMA transfer cycle time per word. 15-0 Cycle time in ns.
66	0078h	2	F	Recommended Multiword DMA transfer cycle time. 15-0 Cycle time in ns.
67	0078h	2	F	Minimum PIO transfer cycle time without flow control. 15-0 Cycle time in ns.
68	0078h	2	F	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in ns.
69-70	0000h	4	F	Reserved
71-74	0000h	8	F	Reserved for Identify Packet Device Command
75	0000h	2	F F	Queue depth 15-5 Reserved 4-0 Maximum queue depth - 1
76	0206h	2	F F F F F F F F	Serial ATA Capabilities 15-11 Reserved for Serial ATA 10 1: supports PHY Event Counts 9 1: supports receipt of Host initiated power management requests 8 1: supports NCQ Feature Set 7-3 Reserved for Serial ATA 2 1: supports SATA Gen2 Signaling Speed (3.0Gb/s) 1 1: supports SATA Gen1 Signaling Speed (1.5Gb/s) 0 Shall be cleared to zero
77	0000h	2	X	Reserved for Serial ATA
78	0008h	2	F F F F F F F F	Serial ATA Feature Supported 15-7 Reserved for Serial ATA 6 1: supports Software Settings Preservation 5 Reserved for Serial ATA 4 1: supports in-order data delivery 3 1: supports initiating power management 2 1: Supports DMA setup auto-activation 1 1: Supports none-zero buffer offset 0 Shall be cleared to zero
79	0000h	2	F F F F F F F F	Serial ATA Feature Enabled 15-7 Reserved for Serial ATA 6 1: Software Settings Preservation enabled 5 Reserved for Serial ATA 4 1: In-order data delivery enabled 3 1: Initiating power management enabled 2 1: DMA setup auto-activation enabled 1 1: None-zero buffer offset enabled 0 Shall be cleared to zero
80	01FCh	2	F F F F F	Major version number, ATA-8 support 15 Reserved 14 Reserved for ATA/ATAPI-14 13 Reserved for ATA/ATAPI-13 12 Reserved for ATA/ATAPI-12 11 Reserved for ATA/ATAPI-11 10 Reserved for ATA/ATAPI10

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information
			F	9 Reserved for ATA/ATAPI-9
			F	8 1: supports ATA/ATAPI-8
			F	7 1: supports ATA/ATAPI-7
			F	6 1: supports ATA/ATAPI-6
			F	5 1: supports ATA/ATAPI-5
			F	4 1: supports ATA/ATAPI-4
			F	3 Obsolete
			F	2 Obsolete
			F	1 Obsolete
			F	0 Reserved
81	0000h	2	F	Minor version number
82	742Bh	2		Features/command sets supported (NOP, SMART,...)
			X	15 Obsolete
			F	14 1: NOP command supported
			F	13 1: READ BUFFER command supported
			F	12 1: WRITE BUFFER command supported
			X	11 Obsolete
			F	10 1: Host Protected Area feature set supported
			F	9 1: DEVICE RESET command supported
			F	8 1: SERVICE interrupt supported
			F	7 1: release interrupt supported
			F	6 1: look-ahead supported
			F	5 1: write cache supported
			F	4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
			F	3 1: mandatory Power Management feature set supported
			F	2 1: Removable Media feature set supported
			F	1 1: Security Mode feature set supported
			F	0 1: SMART feature set supported
83	7500h	2		Features/command sets supported (Flush Cache, ...)
			F	15 Shall be cleared to zero
			F	14 Shall be set to one
			F	13 Reserved
			F	12 Shall be set to one to indicate that the mandatory FLUSH CACHE command is supported
			F	11 1: DCO feature set is supported
			F	10 1: 48-bit Address feature set is supported
			F	9 1: AAM feature set is supported
			F	8 1: SET MAX security extension supported
			F	7 Reserved
			F	6 1: SET FEATURES subcommand required to spin up after power-up
			F	5 1: Power-Up In Standby feature set supported
			F	4 1: Removable Media Status Notification feature set supported
			F	3 1: Advanced Power Management feature set supported
			F	2 1: CFA feature set supported
			F	1 1: READ/WRITE DMA QUEUED supported
			F	0 1: DOWNLOAD MICROCODE command supported
84	4002h	2		Features/command sets supported (extension)
			F	15 Shall be cleared to zero
			F	14 Shall be set to one
			F	13 1: IDLE IMMEDIATE command with UNLOAD feature is

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information
				supported
			F	12-11 Reserved for 3D NAND
			F	10-9 Obsolete
			F	8 1: 64-bit World wide name is supported
			F	7 1: WRITE DMA QUEUED FUA EXT command is supported
			F	6 1: WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported
			F	5 1: GPL feature set is supported
			F	4 1: Streaming feature set is supported
			F	3 1: Media Card Pass Through Command feature set is supported
			F	2 1: Media serial number is supported
			F	1 1: SMART self-test supported
			F	0 1: SMART error logging supported
85	XXXXh	2		Features/command sets enabled (NOP, SMART,...)
			X	15 Obsolete
			F	14 1: NOP command enabled
			F	13 1: READ BUFFER command enabled
			F	12 1: WRITE BUFFER command enabled
			X	11 Obsolete
			V	10 1: Host Protected Area feature set enabled
			F	9 Shall be cleared to zero to indicate that the DEVICE RESET command is not supported
			V	8 1: SERVICE interrupt enabled
			V	7 1: release interrupt enabled
			V	6 1: look-ahead enabled
			V	5 1: write cache enabled
			F	4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
			F	3 Shall be set to one to indicate that the mandatory Power Management feature is supported
			X	2 Obsolete
			V	1 1: Security feature set enabled
			V	0 1: SMART feature set enabled
86	XXXXh	2		Features/command sets enabled (Flush Cache, ...)
			F	15 1: Word 119-120 are valid
			F	14 Reserved
			F	13 1: FLUSH CACHE EXT command supported
			F	12 1: FLUSH CACHE command supported
			F	11 1: DCO feature set is supported
			F	10 1: 48-bit Address feature set is supported
			V	9 1: AAM feature set is supported
			V	8 1: SET MAX security extension enabled by SET MAX SET PASSWORD
			X	7 Reserved for Address Offset Reserved Area Boot Method
			F	6 1: SET FEATURES subcommand required to spin-up after power-up
			V	5 1: Power-Up In Standby feature set enabled
			X	4 Obsolete
			V	3 1: Advanced Power Management feature set enabled
			F	2 1: CFA feature set is supported
			F	1 1: TCQ feature set is supported
			F	0 1: DOWNLOAD MICROCODE command supported

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information
87	XXXXh	2	F	Features/command sets enabled (extension)
			F	15 Shall be cleared to zero
			F	14 Shall be set to one
			F	13 1: The IDLE IMMEDIATE command with UNLOAD feature is supported
			X	12-11 Reserved for 3D NAND
			X	10-9 Obsolete
			F	8 1: 64-bit World wide name is supported
			F	7 1: WRITE DMA QUEUED FUA EXT command is supported
			F	6 1: WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported
			F	5 1: GPL feature set is supported
			X	4 Obsolete
			V	3 1: Media Card Pass Through Command feature set is supported
			V	2 1: Media serial number is supported
			F	1 1: SMART self-test supported
			F	0 1: SMART error logging supported
88	007Fh	2	F	Ultra DMA Mode Supported and Selected
			F	15 Reserved
			V	14 1: Ultra DMA mode 6 is selected 0: Ultra DMA mode 6 is not selected
			V	13 1: Ultra DMA mode 5 is selected 0: Ultra DMA mode 5 is not selected
			V	12 1: Ultra DMA mode 4 is selected 0: Ultra DMA mode 4 is not selected
			V	11 1: Ultra DMA mode 3 is selected 0: Ultra DMA mode 3 is not selected
			V	10 1: Ultra DMA mode 2 is selected 0: Ultra DMA mode 2 is not selected
			V	9 1: Ultra DMA mode 1 is selected 0: Ultra DMA mode 1 is not selected
			V	8 1: Ultra DMA mode 0 is selected 0: Ultra DMA mode 0 is not selected
			F	7 Reserved
			F	6 1: Ultra DMA mode 6 and below are supported
			F	5 1: Ultra DMA mode 5 and below are supported
			F	4 1: Ultra DMA mode 4 and below are supported
			F	3 1: Ultra DMA mode 3 and below are supported
			F	2 1: Ultra DMA mode 2 and below are supported
			F	1 1: Ultra DMA mode 1 and below are supported
			F	0 1: Ultra DMA mode 0 is supported
89	0003h	2	X	15-8 Reserved
			F	7-0 Time required for security erase unit completion
90	0000h	2	X	15-8 Reserved
			F	7-0 Time required for Enhanced security erase completion
91	0000h	2	V	Current advanced power management value
92	FFFEh	2	V	Master Password Identifier
93-99	0000h	14	X	Reserved
100-103	VVVVh	8	V	Total Number of User Addressable Logical Sectors for 48-bit commands (QWord)
104-127	0000h	48	V	Reserved
128	0001h	2		Security status

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information
			F	15-9 Reserved
			V	8 Security level 0: High, 1: Maximum
			X	7-6 Reserved
			F	5 1: Enhanced security erase supported
			V	4 1: Security count expired
			V	3 1: Security frozen
			V	2 1: Security locked
			V	1 1: Security enabled
			F	0 1: Security supported
129-159	0000h	62	X	Reserved for vendor
160	0000h	2		CFA power mode
			F	15 Word 160 supported
			X	14 Reserved
			F	13 CFA power mode 1 is required for one or more commands implemented by the device
			V	12 CFA power mode 1 disabled
			F	11-0 Maximum current in mA
161-175	0000h	30	X	Reserved for Compact Flash Association
176-216	0000h	82	V	Reserved
217	0001h	2	F	Nominal media rotation rate
218-254	0000h	74	X	Reserved
255	VVVVh	2		Integrity Word
			V	15-8 Checksum
			V	7-0 Signature

NOTICE:

1. F/V: Fixed/Variable content.
 2. F: The content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
- V: The contents of the word are variable and may change depending on the state of the device or the commands executed by the device.
- X: The content of the word may be fixed or variable.

3.5 Set Feature Command

The table listed below is the supported feature field set in feature register

Table 9 : Feature Field Definitions

Value	Function
02h	Enable volatile write cache
03h	Set transfer mode
05h	Enable the APM feature set
10h	Enable use of SATA feature
55h	Disable read look-ahead feature
66h	Disable reverting t power on defaults by soft reset
82h	Disable volatile write cache
85h	Disable the APM feature set
90h	Disable use of SATA feature
AAh	Enable read look-ahead feature
CCh	Enable reverting to power-on defaults

The effective SATA features are defined as below:

Table 10 : SATA Features

Sector Count Value	Description
02h	DMA Setup FIS Auto-Active optimization
03h	Device-Initiated interface power state transitions
06h	Software Settings Preservation

3.6 SMART Feature Command

SILICON POWER'S mSATA SATA SSD MSA3K0E series supports SMART function. It response the up-to-date SMART command set with the SMART data structure as following:

Table 11 : SMART Feature Registers Values

Value	Command
D0h	SMART Read Data
D1h	Read Attribute Threshold
D2h	SMART Enable/Disable Attribute Autosave
D3h	Save Attribute Values
D4h	Execute Off-Line Immediate
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status
Others	Reserved

Table 12 : Device SMART Data Structure

Offset	Description
0-1	SMAT Structure Revision code
2-361	Attribute entries 1 to 30 (12 bytes each)
362	Off-line data collection status (No off-line data collection) (Fixed)
363	Self-test execution status byte (Self-test completed) (Fixed)
364-365	Total time in seconds to complete off-line data collection activity (Fixed)
366	Reserved
367	Off-line data collection capability (No Off-line data collection) (Fixed)
368-369	SMART capability
370	Error logging capability (No error logging) (Fixed)
371	Reserved
372	Short self-test routine recommended polling time (in minutes) (Fixed)
373	Extended self-test routine recommended polling time (in minutes) (Fixed)
374-510	Reserved
511	Data structure checksum

- (0-1) Revision code

This revision code area defines the firmware revision for the device.

- (2-361) Attribute entries 1 to 30 (12 bytes each)

There are five attributes that are defined for this device. These return their data in the attribute section of the SMART data, using a 12-byte data field. Rest of the area is reserved. The Individual attribute data structure is defined as following:

Smart ID 1Byte	Item Name	Status 2Bytes	Normalize 1Byte	Worst 1Byte	Raw 6Bytes	Threshold 1Byte	Unit
01	Raw data error rate	2Fh	100	100	4Bytes	0	Count/Sector
05	Reallocated sector count	03h	100	100	2Bytes	0	Block
09	Power on hour count	02h	100	100	4Bytes	0	Hours
0C	Power cycle count	03h	100	100	4Bytes	0	Count
A1	GDN	03h	100	100	4Bytes	0	Count
A2	Total erase count	03h	100	100	4Bytes	0	Count
A3	Max PE cycle	03h	100	100	4Bytes	0	Count
A4	Average erase count	03h	100	100	4Bytes	0	Count
A6	Total bad block count	03h	100	100	4Bytes	0	Count
A7	SSD protect mode	03h	100	100	4Bytes	0	ON / OFF
A8	SATA Phy error count	03h	100	100	4Bytes	0	Count
A9	Health	03h	100	100	4Bytes	0	Count
AB	Program fail count	03h	100	100	4Bytes	0	Count
AC	Erase fail count	03h	100	100	4Bytes	0	Count
AE	Unexpected power loss count	03h	100	100	4Bytes	0	Count
AF	ECC fail count	03h	100	100	4Bytes	0	Count
B5	Unaligned access count	03h	100	100	4Bytes	0	Count
BB	Reported uncorrectable error	03h	100	100	4Bytes	0	Count
C2	Enclosure temperature	03h	100	100	4Bytes	0	°C
C3	Cumulative corrected ecc	03h	100	100	4Bytes	0	Count/Sector
C4	Reallocation event count	03h	100	100	4Bytes	0	Count
C7	Ultra DMA CRC error count	03h	100	100	4Bytes	0	Count
CE	Min. erase count	03h	100	100	4Bytes	0	Count
CF	Max erase count	03h	100	100	4Bytes	0	Count
E8	Available reserved space	03h	100	100	4Bytes	0	Percentage
E9	Vendor Specific	03h	100	100	4Bytes	0	Count
F1	Write life time	03h	100	100	4Bytes	0	GB

F2	Read life time	03h	100	100	4Bytes	0	GB
F9	Total GB written to NAND (TLC)	03h	100	100	4Bytes	0	GB
FA	Total GB written to NAND (SLC)	03h	100	100	4Bytes	0	GB

- (368-369) SMART capabilities

The following describes the definition for the SMART capabilities bits.

- Bit 0 - If this bit is set to one, the device saves SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode. If this bit is cleared to zero, the device does not save SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode.
- Bit 1 - This bit shall be set to one to indicate that the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.
- Bits (15:2) (Reserved).

- (372-373) Self-test routine recommended polling time

The self-test routine recommended polling time shall be equal to the number of minutes that is the minimum recommended time before which the host should first poll for test completion status. Actual test time could be several times this value. Polling before this time could extend the self-test execution time or abort the test depending on the state of bit 2 of the off-line data capability bits.

- (511) Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

4. Ordering Information

4.1 Part Number Definition

Table 13 : Part Number Definition

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	S	P	0	1	0	T	I	M	D	A	3	K	5	E	V	0
Code 1-2: Brand	SP: Silicon Power															
Code 3-6: Capacity	032G: 32GB; 064G: 64GB; 128G: 128GB; 256G: 256GB; 512G: 512GB; 010T: 1TB															
Code 7: Product	I: Industrial Grade Product															
Code 8-10: Type & Form Factor	MDA: SATA M.2 2242															
Code 11-13: Model Series	3K5 Series: WD (3D TLC)															
Code 14: SSD Series	E: SSD without DRAM															
Code 15: Operation Temperature	V: Normal temperature -20°C to +75°C															
Code 16: Reserved	0: Standard															

4.2 Standard M.2 2242 SATA SSD MDA3K0E Series Information

Capacity	Part Number	BOM Code	Description	R/W Performance	
				Maximum (MB/s)	IOPS
Normal Temperature (-20°C ~ 75°C)					
32GB	SP032GIMDA3K5EV0	032GIMDA3K5EV0-020	BiCS4 256Gb*1	230 / 160	10K / 19K
64GB	SP064GIMDA3K5EV0	064GIMDA3K5EV0-020	BiCS5 512Gb*1	295 / 240	9K / 41K
64GB	SP064GIMDA3K5EV0	064GIMDA3K5EV0-030	BiCS4 256Gb*2	295 / 240	9K / 41K
64GB	SP064GIMDA3K5EV0	064GIMDA3K5EV0-040	BiCS5 512Gb*1	295 / 240	9K / 54K
128GB	SP128GIMDA3K5EV0	128GIMDA3K5EV0-030	BiCS5 1Tb*1	545 / 495	17K / 51K
128GB	SP128GIMDA3K5EV0	128GIMDA3K5EV0-040	BiCS5 1Tb*1	540 / 480	18K / 67K
256GB	SP256GIMDA3K5EV0	256GIMDA3K5EV0-020	BiCS5 1Tb*2	545 / 520	33K / 55K
256GB	SP256GIMDA3K5EV0	256GIMDA3K5EV0-030	BiCS5 1Tb*2	545 / 520	31K / 67K
512GB	SP512GIMDA3K5EV0	512GIMDA3K5EV0-020	BiCS5 2Tb*2	545 / 520	48K / 61K
512GB	SP512GIMDA3K5EV0	512GIMDA3K5EV0-030	BiCS5 2Tb*2	545 / 520	44K / 68K
010TB	SP010TIMDA3K5EV0	010TIMDA3K5EV0-010	BiCS5 4Tb*2	545 / 520	50K / 65K

010TB	SP010TIMDA3K5EV0	010TIMDA3K5EV0-020	BiCS5 4Tb*2	540 /515	44K / 69K
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4.3 Appendix

Table 14 : Abbreviation

Item	Abbreviation	Description
1	PCIe	Peripheral Component Interconnect Express
2	NVMe	Non-Volatile Memory Express
3	Gen	Generation
4	TBE	Tera Byte Write
5	MTBF	Mean Time Between Failures
6	LDPC	Low Density Parity Check
7	RAID	Redundant Array of Independent Drives
8	ECC	Error Correction Code
9	TCG	Trusted Computing Group
10	SMART	Self-Monitoring Analysis and Reporting Technology
11	FDE	Full Disk Encryption
12	AES	Advanced Encryption Standard
13	SLC	Single-Level Cell
14	SSD	Solid State Disk
15	OP	Over Provisioning
16	PS	Power Shield
17	DC	Direct Current
18	LED	Light Emitting Diode
19	DRAM	Dynamic Random Access Memory
20	PE	Program/Erase
21	EAF	Write Amplification Factor
22	ELE	Wear Leveling Efficiency
23	Ta	Ambient Temperature
24	LBA	Logical Block Address

Contact Information

Silicon Power Computer & Communications Incorporation, a solid state memory or storage business company, provides total solutions in the design and marketing of SSD, Flash Module, and Industry Card products. For further supporting or detail information related to the products, please inform us through the following contact email address: isupport@silicon-power.com. We will response the requests soon.